Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A read/write device for a disk drive, having a pre-amplifier and a recording head, comprising:

a write signal path between said pre-amplifier and said recording head, said write signal path having a write current;

a read signal path between said pre-amplifier and said recording head, said read signal path having an induced current related to said write current; and

a shunt path in said pre-amplifier to draw a part of said induced current from said read signal path.

2. (Original) The read/write device of claim 1, further comprising a sensor in said recording head coupled to said read signal path.

3. (Original) The read/write device of claim 2, wherein said induced current generates a sensor current of about 0.25 milliamps.

4. (Original) The read/write device of claim 1, further comprising a read amplifier in said pre-amplifier.

5. (Currently amended) The read/write device of claim [[3]] 4, wherein said shunt path is coupled between said read signal path and said read amplifier.

6. (Original) The read/write device of claim 1, wherein said shunt path includes a set of transmission gates.

7. (Original) The read/write device of claim 6, wherein said set of transmission gates includes a first transistor and a second transistor.

8. (Original) The read/write device of claim 7, wherein said first transistor is an n-channel transistor.

9. (Original) The read/write device of claim 7, wherein said second transistor is a p-channel transistor.

10. (Original) The read/write device of claim 6, wherein said set of transistors has a low drain-to-source channel resistance.

11. (Original) The read/write device of claim 1, wherein said shunt path has a resistance of about 10 ohms.

12. (Original) The read/write device of claim 1, wherein said pre-amplifier includes a write driver to generate said write current in said write signal path.

13. (Original) The read/write device of claim 10, wherein said write driver generates an electric field.

14. (Original) The read/write device of claim 10, wherein said write current generates a magnetic field.

15. (Original) A read/write device, comprising:

a write signal path having a write current, said write current to induce an induced current in a read signal path; and

a shunt path to shunt said induced current from said read signal path.

16. (Original) The read/write device of claim 15, further comprising a sensor coupled to said read signal path.

17. (Original) The read/write device of claim 15, wherein said shunt path comprises two transmission gates.

18. (Original) The read/write device of claim 15, wherein said shunt path has a resistance below about 10 ohms.

19. (Original) The read/write device of claim 15, wherein said shunt path couples said read signal path to a read amplifier.

20. (Original) A method for limiting a sensor current in a magneto-resistive sensor, comprising:

inducing a current in a read signal path coupled to said sensor; and

shunting said current from said read signal path with a shunt path, wherein said shunt path is opposite said sensor on said read signal path; and

inducing a voltage in a read signal path coupled to said sensor; and

shunting the current that is generated due to said voltage from said read signal path, wherein said shunt path is opposite said sensor on said read signal path.

21. (Original) The method of claim 20, further comprising generating a write current in a write signal path.

22. (Original) The method of claim 21, further comprising generating an electric field about said write signal path, said electric field inducing said current.

23. (Currently amended) The method of claim 21, further comprising generating a magnetic field about said write signal path, said magnetic field inducing a voltage potential.

24. (Original) The method of claim 20, further comprising transmission gates within said shunt path.

25. (Currently amended) The method of claim [[20]] 24, further comprising saturating transistors within said transmission gates.